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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/017,232	12/13/2001	Michael Charles LaCroix	104427-100	1610

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EXAMINER
GLASS, ERICK DAVID

ART UNIT	PAPER NUMBER
2837	

DATE MAILED: 12/15/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/017,232	LACROIX, MICHAEL CHARLES	
	Examiner	Art Unit	
	Erick Glass	2837	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 January 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☒ Claim(s) *19 and 20* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 January 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

Applicant's arguments filed January 13, 2006 have been fully considered but they are not persuasive.

In response to applicant's argument (A) that the examiner's conclusion of obviousness is based upon improper hindsight reasoning, it must be recognized that any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made, and does not include knowledge gleaned only from the applicant's disclosure, such a reconstruction is proper. See *In re McLaughlin*, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971).

In response to applicant's argument (A & F) that the examiner has combined an excessive number of references, reliance on a large number of references in a rejection does not, without more, weigh against the obviousness of the claimed invention. See *In re Gorman*, 933 F.2d 982, 18 USPQ2d 1885 (Fed. Cir. 1991).

With respect to arguments A and C, that the Prior Art does not teach every aspect of the invention, specifically monitoring the voltage across the motor, Pedrazzani teaches voltage being monitored at VSN and VSP. The measurement is taken from the resistor which is know in the art to be a voltage sensor to determine the voltage drop across the motor. The applicant determines the applied voltage in the same manner according to his specification and drawings (pg 7, lines 18-25). VSN and VSP are inputted to the sensing amplifier (fig. 4, 44) to determine the voltage.

The motivation to combine the state machine of Eroglu into the circuit of Pedrazzini is that they are both control unit (control logic, chips, processor, etc.) and equivalents, easily replaced with hardware (para. 0045).

Claim Rejections - 35 USC § 112

Claim 15, rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The amended claim 15, originally stated, "a digital to analog converter means, a digital signal to analog voltage for setting a voltage across the electric motor", and now also includes " the microprocessor and associated digital memory for setting the voltage supplied to the electric motor." The statement is contradicting, and unclear of what mechanism carries out the particular process.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 10, and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pedrazzini et al. (6,693,400), Sato et al. (5,315,458) and Eroglu et al. (2002/0084758).

With respect to claim 1, Pedrazzini et al. discloses an electric motor controller, comprising: a digital to analog converter means for setting voltage across a motor (Fig. 4, #34 controls #32 to set the voltage across the motor); a control circuit for converting a duty cycle of an input signal for output to the digital to analog converter means (Fig. 4, 64 converts the duty cycle of the ADCIN signal and outputs it to #46 along with the output of #48),. and a closed loop feedback loop means for monitoring and setting the voltage across the motor (Fig. 4, measured voltage input to #32 at VSN and VSP).

Pedrazzini et al. does not disclose an 8-bit DAC, a state machine, and does not explicitly disclose setting a voltage across a motor.

Sato et al. discloses driving a motor where a signal is converted to an analog voltage signal, amplified, and sent to drive the motor as the voltage across the motor (col. 6, lines 9-17; Fig. 8, output of #80 is a voltage signal; voltage signal amplified by #82 and sent directly to the motor). The motivation to use a voltage signal is because this signal is used with a power amplifier.

Eroglu et al. discloses a microprocessor (controller logic circuit) and associated memory that controls a state machine (Fig. 2, #s 26 and 27). Additionally, Eroglu et al. teaches that a portion of a motor control circuit can be implemented using a state machine (para. 0045). The motivation to use implement a state machine to replace a portion of the motor control circuitry is so that portion can be implemented in hardware (para. [0045], since general disclosure of a state machine, this implies the state machine could be.

digital).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of the invention that the amplifier of Pedrazzini et al. would output a voltage signal to set the voltage across the motor based on the teachings of Sato et al. This would provide the advantage of allowing a circuit designer the ability of using a power amplifer to amplify the voltage signal, as taught by Sato et al. Additionally, it would have been obvious to one having ordinary skill in the art at the time of the invention that the controller chip and driver chip of Pedrazzini et al. could be replaced by a microcomputer (including memory) and state machine, thus making the state machine set the voltage across the motor, which would provide the advantage of allowing the circuitry to be implemented in hardware, as taught by Eroglu et al. Finally, with respect to the 8-bit feature, the examiner takes Official Notice. Pedrazzini et al. discloses a DAC (Fig. 4, #46) but does not disclose its resolution capabilities. It would have been obvious to one having ordinary skill in the art at the time of the invention that the DAC of Pedrazzini et al. would be and 8-bit DAC. The motivation to use an 8-bit DAC is because it provides better resolution than would lower bit DAC.

With respect to claims 10 and 11, Pedrazzini et al. disclose the system comprising a component/electric motor (Fig. 4, #28).

Claims 2, 3, 10, 12, 13, and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pedrazzini et al., Sato et a1., and Eroglu et al. as applied to claim 1 above, and further in view of Maxwell, Jr. et al. (6,8 16,758).

Pedrazzini et al., Sato et al., and Eroglu et al. do not disclose an over-current sense circuit (claims 2 and 13), an over/under voltage sense circuit (claims 3 and 14), and a component being an electric light (claims 10 and 12).

Maxwell, Jr. et al. discloses a controller for a load that has both an over-current sense circuit and an over/under voltage sense circuit (Fig. 2, #s 32 and 30). The motivation to use an over-current sense circuit and an over/under voltage sense circuit is to protect the motor (col. 9,lines 39-55). Additionally, with respect to claims 10 and 12, first note that for claim 10, the examiner has redefined "a component." Here, Maxwell, Jr. teaches that a controller can be used with many loads (components). Furthermore, Maxwell, Jr. states that the system is used to power one or more electrical components in airplanes and automobiles, including electric motors and servos, and various other electrical systems (cols. 6/7, lines 65-67/1-42). Because Maxwell, Jr. discloses using a controller system to control various electrical systems in airplanes and automobiles, it would have been obvious to one having ordinary skill in the art at the time of the invention that the Maxwell, Jr. disclosure includes lighting systems in airplanes and automobiles, which would include an electric light.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of the invention to implement into the circuit of Pedrazzini et al; an over-current sense circuit and an over/under voltage sense circuit, thereby providing the advantage of protecting the load from damage due to excessive current and/or voltage, as taught by Maxwell, Jr. et al. Additionally, it would have been obvious to one having ordinary skill in the art at the time of the invention that the system of Pedrazzini et al. could be used to control either a motor and a light system because Maxwell, Jr. teaches that controllers may be used to control multiple systems within airplanes and automobiles, including an electric light in a lighting system.

Claims 4, 5, 6, 7, 9, and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pedrazzini et al. (6,693,400), Sato et al. (5,315,458) and Eroglu et al. (2002/0084758).

With respect to claim 4, Pedrazzini et al. disclose a circuit arrangement for an electric motor controller, comprising: a controller logic circuit that controls a driver circuit to set the voltage across an electric motor (Fig. 4, #34 controls #32 to set the voltage across the motor; and a closed loop feedback circuit for generating a signal indicating the voltage across the electric motor, the signal being input to the driver circuit for monitoring (Fig. 4, measured voltage input to #32 at VSN and VSP), the signal being for comparison to the voltage set (fig. 4, 44).

With respect to claim 15, (as best understood interpretation of the claimed language) Pedrazzini et al. discloses a system for controlling the speed of an electric motor, comprising; a digital to analog converter means for setting a voltage across the electric motor (Fig. 4,#46); a controller that generates the digital signal (Fig. 4, output of #48 is a digital signal; Fig. 12A, #78; see also col. 4, lines 44-48; where instructions from software implies memory) to control a driver circuit for converting the duty cycle of an input signal (Fig. 4, #38 converts the duty cycle of the input signal PSMA to control the output signal OUTA; see also col. 3, lines 17- 19; PSM has a duty cycle), and where the driver circuit sets the voltage supplied to the electric motor (Fig. 4, #38 sets the voltage to #28); and a closed loop feedback means adapted and configured to monitor the voltage across the motor and generates a signal for input to the micro-controller (Fig. 4, measured voltage input to #32 at VSN and VSP).

With respect to claims 4 and 15, Pedrazzini et al. does not disclose a microprocessor, a state machine, and does not explicitly disclose setting a voltage across the motor.

Sato et al. discloses driving a motor where a signal is converted to an analog voltage signal, amplified, and sent to drive the motor as the voltage across the motor (col. 6, lines 9-17; Fig. 8, output of #80 is a voltage signal; voltage signal amplified by #82 and sent directly to the

motor). The motivation to use a voltage signal is because this signal is used with a power amplifier.

With respect to claims 7 and 15, Eroglu et al. discloses a microprocessor (controller logic circuit) and associated memory that controls a state machine (Fig. 2, #s 26 and 27). Additionally, Eroglu et al. teaches that a portion of a motor control circuit can be implemented using a state machine (para. [0045], since general disclosure of a state machine, this implies the state machine could be digital). The motivation to use implement a state machine to replace a portion of the motor control circuitry is so that portion can be implemented in hardware (para. [0045]).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of the invention that the amplifier of Pedrazzini et al. would output a voltage signal to set the voltage across the motor based on the teachings of Sato et al. This would provide the advantage of allowing a circuit designer the ability of using a power amplifier to amplify the voltage signal, as taught by Sato et al. Additionally, it would have been obvious to one having ordinary skill in the art at the time of the invention that the controller chip and driver chip of Pedrazzini et al. could be replaced by a microcomputer (including memory) and state machine, thus making the state machine set the voltage across the motor, which would provide the advantage of allowing the circuitry to be implemented in hardware, as taught by Eroglu et al.

With respect to claim 5, since Eroglu et al. disclose implementing a state machine, the state machine controls the spin-up routine, which is interpreted as a running state (para. [0045]).

With respect to claim 6, since Eroglu et al. teaches replacing portions of a control circuit for a motor with a state machine, this means that the state machine has a lockout state (Fig. 3, #35 and subsequent steps).

With respect to claim 9, Pedrazzini et al. disclose the circuit arrangement being directly coupled to the electric motor (Fig. 4, #28 to circuit arrangement #s 34, 32, R1, R2, R3, C3).

Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Pedrazzini et al. (6,693,400), Sato et al. (5,315,458), and Eroglu et al. (2002/0084758) as applied to claim 4 above.

Pedrazzini et al., Sato et al., and Eroglu et al. do not disclose an 8-bit DAC.

With respect to this feature, the examiner takes Oxcial Notice. Pedrazzini et al. discloses a DAC (Fig. 4, #46) but does not disclose its resolution capabilities. It would have been obvious to one having ordinary skill in the art at the time of the invention that the DAC of Pedrazzini et al. would be and 8-bit DAC. The motivation to use an 8-bit DAC is because it provides better resolution than would lower bit DAC.

Claims 16 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pedrazzini et al. (6,693,400), Sato et al. (5,315,458) and Eroglu et al. (2002/0084758) as applied to claim 15 above.

Eroglu et al. discloses a control device used with CD ROM drives, but Eroglu et al., Pedrazzini et al., and Sato et al. do not disclose an automobile comprising the system of claim 15.

With respect to this feature, the examiner takes Official Notice. Eroglu et al. discloses a system that controls CD ROM drivers. It would have been obvious to one having ordinary skill

in the art at the time of the invention that the system of Pedrazzini et al., Sato et al., and Eroglu et al., can be used in an automobile because automobiles are equipped with CD ROM drivers so passengers can watch for instance movies.

With respect to claim 17, Pedrazzini et al. disclose the system being a temperature control system (col. 4, lines 57-59).

Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Pedrazzini et al. (6,693,400), Sato et al. (5,315,458), Eroglu et al. (2002/0084758), and Maxwell, Jr. et al. (6,816,758).

With respect to claim 18, Pedrazzini et al. discloses a controller for an electric motor, comprising: a driver circuit for converting the duty cycle of an input signal generated by an associated closed loop feedback loop (Fig. 4, #38 converts the duty cycle of the input signal PSMA to control the output signal OUTA; see also col. 3,lines 17-19; PSM has a duty cycle; associated with feedback from ADCIN and C3 and R3); a digital to analog converter for setting voltage across the electric motor (Fig. 4, #46 sets voltage across #28); and the closed loop feedback further adapted to and configured to monitor the voltage across the motor and generates the input signal to the digital state machine (Fig. 4, measured voltage input to #32 at VSN and VSP).

Pedrazzini et al. does not disclose a state machine, an over-current sense circuit, over/under voltage sense circuit, an 8-bit DAC, and does not explicitly disclose setting a voltage across the motor.

Sato et al. discloses driving a motor where a signal is converted to an analog voltage signal, amplified, and sent to drive the motor as the voltage across the motor (col. 6,lines 9-17;

Fig. 8, output of #80 is a voltage signal; voltage signal amplified by #82 and sent directly to the motor). The motivation to use a voltage signal is because this signal is used with a power amplifier.

Eroglu et al. discloses a microprocessor (controller logic circuit) and associated memory that controls a state machine (Fig. 2, #s 26 and 27).

Additionally, Eroglu et al. teaches that a portion of a motor control circuit can be implemented using a state machine (para. [0045], since general disclosure of a state machine, this implies the state machine could be digital). The motivation to use implement a state machine to replace a portion of the motor control circuitry is so that portion can be implemented in hardware (para. [0045]).

Maxwell, Jr. et al. discloses a controller for a load that has both an over-current sense circuit and an over/under voltage sense circuit (Fig. 2, #s 32 and 30). The motivation to use an over-current sense circuit and an over/under voltage sense circuit is to protect the motor (col. 9,lines 39-55).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of the invention that the amplifier of Pedrazzini et al. would output a voltage signal to set the voltage across the motor based on the teachings of Sato et al. This would provide the advantage of allowing a circuit designer the ability of using a power amplifier to amplify the voltage signal, as taught by Sato et al. Additionally, it would have been obvious to one having ordinary skill in the art at the time of the invention that the controller chip and driver chip of Pedrazzini et al. could be replaced by a microcomputer (including memory) and state machine, thus making the state machine set the voltage across the motor, which would provide the advantage of allowing

the circuitry to be implemented in hardware, as taught by Eroglu et al. Also, it would have been obvious to one having ordinary skill in the art at the time of the invention to implement into the circuit of Pedrazzini et al., an over-current sense circuit and an over/under voltage sense circuit, thereby providing the advantage of protecting the load from damage due to excessive current and/or voltage, as taught by Maxwell, Jr. et al. Finally, With respect to the 8-bit DAC, the examiner takes Official Notice. Pedrazzini et al. discloses a DAC (Fig. 4, #46) but does not disclose its resolution capabilities. lt would have been obvious to one having ordinary skill in the art

at the time of the invention that the DAC of Pedrazzini et al. would be and 8-bit DAC. The motivation to use an 8-bit DAC is because it provides better resolution than would lower bit DAC.

Claims 19-20 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Prior Art

Mazda (6,140,784) disclose an H-bridge driver that controls the direction of current to the VCM and the magnitude of voltage-across the VCM.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO

MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Erick Glass whose telephone number is 571-272-8395. The examiner can normally be reached on 8-5 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lincoln Donovan can be reached on 571-272-1988. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

EG

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SUPERVISORY PATENT EXAMINER